? show files

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File 348:EUROPEAN PATENTS 1978-201011
         (c) 2010 European Patent Office
File 349:PCT FULLTEXT 1979-2010/UB=20100311|UT=20100304
         (c) 2010 WIPO/Thomson
```

? ds

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Set     Items   Description
S1     569563   (ADDRESS? ? OR LINK OR (WEB OR FTP OR WWW OR HTTP)(1W)SERV-
              ER? ? OR NAME? ?(1N)SERVER? ? OR DNS OR (IP OR INTERNET()PROT-
              OCOL)()ADDRESS?? OR (HOST OR DOMAIN)()NAME? ? OR SERVER()(ID -
              OR IDENTIFICATION))
S2       4323   S1(3N)(BACKUP OR BACK()UP OR SECONDARY OR REDUNDANT)
S3     126871   (POSITION? ?  OR LOCATION? ?  OR OFFSET OR OFF()SET)(3N)(F-
              IELD? ? OR ARRAY? ? OR STORAGE? ? OR MEMORY OR MEMORIES OR ME-
              DIA OR MEDIUM OR MEDUIM)
S4      77464   S1(3N)(MULTI OR MANY OR TWO OR MULTIPL? OR SEVERAL OR MANY
              OR PLURAL? OR RANGE? ? OR ASSORT? OR SERIES OR VARIOUS OR MOR-
              E(3W)(ONE OR 1))
S5        941   S3(10N)S4
S6          8   S5(20N)S2
S7         12   S5(100N)S2
S8          9   S7 AND PY=1963:2003
```

?

Subject summary

? t/ 3,k/ all

Dialog eLink: Order File History

DIALOG(R)File 348: EUROPEAN PATENTS

8/3K/1 (Item 1 from file: 348)
01195120

REPLICABLE PROBE ARRAY
REPLIZIERBARER PROBEN-ARRAY
RESEAU DE SONDES REPLICABLES

Patent Assignee:

- **SurModics, Inc.** (975075)
  9924 West 74th Street; Eden Prairie, MN 55344 (US)
  (Proprietor designated states: all)

Inventor:

- **GUIRE, Patrick, E.**
  6741 Tartan Curve; Eden Prairie, MN 55346; (US)
- **SWANSON, Melvin, J.**
  5290 Mount Carmel Road; Carver, MN 55315; (US)

Legal Representative:

- **Vidon, Patrice (73594)**
  Cabinet Vidon 16 B, rue Jouanet - B.P. 90333 Technopole Atalante; 35703 Rennes Cedex 7; (FR)

	Country	Number	Kind	Date	
Patent	EP	1147222	A1	20011024	(Basic)
Patent	EP	1147222	B1	20061122	
	WO	2000044939		20000803	
Application	EP	2000905741		20000127	
	WO	2000US1944		20000127	
Priorities	US	240466		19990129	

Designated States:
AT; BE; CH; CY; DE; DK; ES; FI; FR; GB;
GR; IE; IT; LI; LU; MC; NL; PT; SE

Extended Designated States:
AL; LT; LV; MK; RO; SI

International Patent Class (V7): C12Q-001/68; B01J-019/00

International Classification (Version 8) IPC	Level	Value	Position	Status	Version	Action	Source	Office
C12Q-0001/68	A	I	F	B	20060101	20000808	H	EP
B01J-0019/00	A	I	L	B	20060101	20000808	H	EP

NOTE: No A-document published by EPO
Language Publication: English
Procedural: English
Application: English

Fulltext Availability Available Text	Language	Update	Word Count
CLAIMS B	(English)	200647	429
CLAIMS B	(German)	200647	406
CLAIMS B	(French)	200647	492
SPEC B	(English)	200647	11320
Total Word Count (Document A) 0			
Total Word Count (Document B) 12647			
Total Word Count (All Documents) 12647			

Specification: ...surface.

In a particularly preferred embodiment of the invention, the master array support surface contains **redundant address** oligonucleotides immobilized thereon, such that a particular **address** appears at a **plurality** of spatially-defined **locations** on the master **array**. As a result of this redundancy, a particular multi-ligand conjugate containing the complementary sequence...

Dialog eLink: Order File History

DIALOG(R)File 348: EUROPEAN PATENTS

8/3K/2 (Item 2 from file: 348)
01152565

REDUNDANT FORM ADDRESS DECODER FOR MEMORY SYSTEM
DEKODER FUR REDUNDANTE ADRESSEN EINES SPEICHERSYSTEMS
DECODEUR D'ADRESSE A FORME REDONDANTE POUR SYSTEME DE MEMOIRE

Patent Assignee:

- **INTEL CORPORATION** (322932)
  2200 Mission College Boulevard, P.O. Box 58119; Santa Clara, CA 95052-8119 (US)
  (Proprietor designated states: all)

Inventor:

- **SAGER, David, J.**
  9540 N.W. Skyview Drive; Portland, OR 97231; (US)

Legal Representative:

- **Wombwell, Francis et al (46022)**
  Potts, Kerr & Co. 15, Hamilton Square; Birkenhead Merseyside CH41 6BR; (GB)

	Country	Number	Kind	Date	
Patent	EP	1129409	A2	20010905	(Basic)
Patent	EP	1129409	B1	20041124	
	WO	2000017757		20000330	
Application	EP	99965886		19990827	
	WO	99US27873		19990827	
Priorities	US	148314		19980904	

Designated States:
DE; GB

International Patent Class (V7): G11C-008/08; G11C-008/10
NOTE: No A-document published by EPO
Language Publication: English
Procedural: English
Application: English

Fulltext Availability Available Text	Language	Update	Word Count
CLAIMS B	(English)	200448	592
CLAIMS B	(German)	200448	570
CLAIMS B	(French)	200448	705
SPEC B	(English)	200448	4564
Total Word Count (Document A) 0			
Total Word Count (Document B) 6431			
Total Word Count (All Documents) 6431			

Claims: ...each memory line associated with an address of a predetermined width, the method comprising:

receiving **redundant** form **address** data for each bit **position** of the **memory address** and at least **two** bit positions below a least significant bit **position** of the **memory address**,

decoding the **redundant** form **address** data, and

driving a first block and a second block (623, 624) based on the... ...memory lines are organized into chunks (625-628) within the blocks (623, 624), and the **redundant** form **address** data at the two bit positions represent an addressed chunk.

17. The method of claim...

Dialog eLink: Order File History

DIALOG(R)File 348: EUROPEAN PATENTS

8/3K/3 (Item 3 from file: 348)
00306062

Digital data processing system.
Digitales Datenverarbeitungssystem.
Systeme du traitement de donnees numeriques.

Patent Assignee:

- **DATA GENERAL CORPORATION** (410940)
  Route 9; Westboro Massachusetts 01581 (US)
  (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)

Inventor:

- **Bratt, Richard Glenn**
  9 Brook Trail Road; Wayland Massachusetts 01778; (US)
- **Clancy, Gerald F.**
  13069 Jaccaranda Center; Saratoga California 95070; (US)
- **Gavrin, Edward S.**
  Beaver Pond Road RFD 4; Lincoln Massachusetts 01773; (US)
- **Gruner, Ronald Hans**
  112 Dublin Wood Drive; Cary North Carolina 27514; (US)
- **Mundie, Craig James**
  136 Castlewood Drive; Cary North Carolina; (US)
- **Schleimer, Stephen I.**
  1208 Ellen Place; Chapel Hill North Carolina 27514; (US)
- **Wallach, Steven J.**
  12436 Green Meadow Lane; Saratoga California 95070; (US)

Legal Representative:

- **Robson, Aidan John et al (69471)**
  Reddie & Grose 16 Theobalds Road; London WC1X 8PL; (GB)

	Country	Number	Kind	Date	
Patent	EP	300516	A2	19890125	(Basic)
Patent	EP	300516	A3	19890426	
Patent	EP	300516	B1	19931124	
Application	EP	88200921		19820521	
Priorities	US	266413		19810522	
	US	266539		19810522	
	US	266521		19810522	
	US	266415		19810522	
	US	266409		19810522	
	US	266424		19810522	

	Country	Number	Kind	Date
	US	266421		19810522
	US	266404		19810522
	US	266414		19810522
	US	266532		19810522
	US	266403		19810522
	US	266408		19810522
	US	266401		19810522
	US	266524		19810522

Designated States:
AT; BE; CH; DE; FR; GB; IT; LI; LU; NL;
SE

Related Parent Numbers: Patent (Application):EP 67556 (EP 823025960)

International Patent Class (V7): G06F-009/46; G06F-012/14; **Abstract Word Count:** 122
Language Publication: English
Procedural: English
Application: English

Fulltext Availability Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1018
CLAIMS B	(German)	EPBBF1	868
CLAIMS B	(French)	EPBBF1	1115
SPEC B	(English)	EPBBF1	154256
Total Word Count (Document A) 0			
Total Word Count (Document B) 157257			
Total Word Count (All Documents) 157257			

Specification: ...following the last pointer to an actual argument, Call Microcode 1001 can now calculate that **location**, convert it into a descriptor, and place it in a FU Register 1004 reserved for...Access Control Lists (ACLs) 1412 are made up of Entries 1414. Each entry two components: **Subject** Template 1416 **and** Mode Specifier 1418. Subject Template 1416 specifies a group of subjects that may reference the Object and Mode Specifier 1418 specifies the kinds of **access** these subjects may have to the Object. Logically speaking, ACL 1412 is checked each time... ...if the modes in the ACL Entry 1414 for the Subject 1408 allow the kind **of** access the process wishes to make. 11. Virtual Processors and Virtual Processor Swapping (Fig. 15...from information belonging to another data channel device. In addition, IOC 1618 may generate overlapping **address** translation Maps for **two** or more data channel devices to allow these data channel devices to share a common ... ...are fill bits.

Bulk data storage in MEM 112 is provided in MSB 1810, which **is** comprised of one **or** more **Memory Array** cards (MAs) 1812. The data path into and out of MA 1812 is through BC...

Dialog eLink: Order File History

DIALOG(R)File 348: EUROPEAN PATENTS

8/3K/4 (Item 4 from file: 348)
00306058

Digital data processing system.
Digitales Datenverarbeitungssystem.
Systeme de traitement de donnees numeriques.

Patent Assignee:

- **DATA GENERAL CORPORATION** (410940)
  Route 9; Westboro Massachusetts 01581 (US)
  (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)

Inventor:

- **Bachman, Brett L.**
  214 W. Canton Street Suite 4; Boston Massachusetts 02116; (US)
- **Bernstein, David H.**
  41 Bay Colony Drive; Ashland Massachusetts 01721; (US)
- **Bratt, Richard Glenn**
  9 Brook Trail Road; Wayland Massachusetts 01778; (US)
- **Clancy, Gerald F.**
  13069 Jaccaranda Center; Saratoga California 95070; (US)
- **Gavrin, Edward S.**
  Beaver Pond Road RFD 4; Lincoln Massachusetts 01773; (US)
- **Gruner, Ronald Hans**
  112 Dublin Wood Drive; Cary North Carolina 27514; (US)
- **Jones, Thomas M. Jones**
  300 Reade Road; Chapel Hill North Carolina 27514; (US)
- **Katz, Lawrence H.**
  10943 S. Forest Ridge Road; Oregon City Oregon 97045; (US)
- **Mundie, Craig James**
  136 Castlewood Drive; Cary North Carolina; (US)
- **Pilat, John F.**
  1308 Ravenhurst Drive; Raleigh North Carolina 27609; (US)
- **Richmond, Michael S.**
  Fearringtn Post Box 51; Pittsboro North Carolina 27312; (US)
- **Schleimer Stephen I.**
  1208 Ellen Place; Chapel Hill North Carolina 27514; (US)
- **Wallach, Steven J.**
  12436 Green Meadow Lane; Saratoga California 95070; (US)
- **Wallach, Walter, A., Jr.**
  1336 Medfield Road; Raleigh North Carolina 27607; (US)

Legal Representative:

- **Robson, Aidan John et al (69471)**
  Reddie & Grose 16 Theobalds Road; London WC1X 8PL; (GB)

	Country	Number	Kind	Date	
Patent	EP	290111	A2	19881109	(Basic)
Patent	EP	290111	A3	19890503	
Patent	EP	290111	B1	19931222	
Application	EP	88200917		19820521	

	Country	Number	Kind	Date
Priorities	US	266404		19810522

Designated States:
AT; BE; CH; DE; FR; GB; IT; LI; LU; NL;
SE

Related Parent Numbers: Patent (Application): EP 67556 (EP 823025960)

International Patent Class (V7): G06F-009/30; ; **Abstract Word Count:** 123

Language Publication: English
Procedural: English
Application: English

Fulltext Availability Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1044
CLAIMS B	(German)	EPBBF1	890
CLAIMS B	(French)	EPBBF1	1185
SPEC B	(English)	EPBBF1	154314
Total Word Count (Document A) 0			
Total Word Count (Document B) 157433			
Total Word Count (All Documents) 157433			

Specification: ...1416 and Mode Specifier 1418. Subject Template 1416 specifies a group of subjects that may **reference** the Object and Mode Specifier 1418 specifies the kinds of access these subjects may have... ...and Interrupt Line 1504 are hardware devices which produce signals that cause the invocation of **KOS** Microcode 706. Timers 1502 contains **two** timing devices: Interval Timer 1506, which may be set by KOS 706, 710 to signal... ...long as the process is bound to a Virtual Processor 612). Binding is carried out **by** KOS 706, 710 at the request of EOS 704. In Fig. 15, **two** Secure Stack Objects 906 are shown, one belonging to the process to which Virtual Processor...

Dialog eLink: Order File History

DIALOG(R)File 348: EUROPEAN PATENTS

8/3K/5 (Item 5 from file: 348)
00274813

Cache invalidate protocol for digital data processing system.
Protokoll zum Ungultigerklaren eines Cachespeichers fur ein digitales Datenverarbeitungssystem.
Protocole d'invalidation de cache pour un systeme numerique de traitement de donnees.

Patent Assignee:

- **DIGITAL EQUIPMENT CORPORATION** (313080)
  146 Main Street; Maynard, MA 01754 (US)
  (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)

Inventor:

- **Rubinfeld, Paul**
  6 Heard Road; Wayland Massachusetts 01778; (US)

Legal Representative:

- **Mongredien, Andre et al (17412)**
  c/o SOCIETE DE PROTECTION DES INVENTIONS 25, rue de Ponthieu; F-75008 Paris; (FR)

	Country	Number	Kind	Date	
Patent	EP	261029	A2	19880323	(Basic)
Patent	EP	261029	A3	19900523	
Patent	EP	261029	B1	19930811	
Application	EP	87402052		19870915	
Priorities	US	908825		19860918	

Designated States:
AT; BE; CH; DE; ES; FR; GB; GR; IT; LI;
LU; NL; SE

International Patent Class (V7): G06F-012/08; ; **Abstract Word Count:** 100

Language Publication: English
Procedural: English
Application: English

Fulltext Availability	Available Text	Language	Update	Word Count
CLAIMS B		(English)	EPBBF1	1214
CLAIMS B		(German)	EPBBF1	668
CLAIMS B		(French)	EPBBF1	890
SPEC B		(English)	EPBBF1	4246
Total Word Count (Document A) 0				
Total Word Count (Document B) 7018				
Total Word Count (All Documents) 7018				

Specification: ...cache control signal over respective lines of said bus, the method comprising the steps of:

A. receiving the **address** in response to said **address control** signal having **an asserted** condition;

B. determining if a correspondence exits between said received address signals and the contents...
...incremented address in response to a second assertion of the cache control signal while the **address** control signal remains **asserted**;

E. determining if a correspondence exists between said incremented address and the contents of one...

Dialog eLink: Order File History

DIALOG(R)File 348: EUROPEAN PATENTS

8/3K/6 (Item 6 from file: 348)
00212453

Method of relocating data in and extending life of a memory system.
Verfahren zur Datenumsiedlung in einem Speichersystem und zur Lebensdauererweiterung eines solchen Systems.
Methode de relogement de donnees dans et d'extension de duree de vie d'un systeme de memoire.

Patent Assignee:

- **PITNEY BOWES INC.** (244950)
  One Elmcroft; Stamford Connecticut 06926-0790 (US)
  (applicant designated states: CH;DE;FR;GB;IT;LI;NL)

Inventor:

- **Chrosny, Wojciech M.**
  81 Linwood Street; Milford, Conn. 06460; (US)
- **Maybruch, Joel**
  87 Harwood Drive; Danbury, Conn. 06810; (US)

Legal Representative:

- **Lehn, Werner, Dipl.-Ing. et al (7471)**
  Hoffmann, Eitle & Partner Patentanwalte Arabellastrasse 4; W-8000 Munchen 81; (DE)

	Country	Number	Kind	Date	
Patent	EP	226205	A2	19870624	(Basic)
Patent	EP	226205	A3	19880113	
Patent	EP	226205	B1	19921223	
Application	EP	86117469		19861216	
Priorities	US	809454		19851216	

Designated States:
CH; DE; FR; GB; IT; LI; NL

International Patent Class (V7): G06F-011/20; G07B-017/02; **Abstract Word Count:** 165
Language Publication: English
Procedural: English
Application: English

Fulltext Availability	Available Text	Language	Update	Word Count
CLAIMS B		(English)	EPBBF1	3996
CLAIMS B		(German)	EPBBF1	1126
CLAIMS B		(French)	EPBBF1	1499
SPEC B		(English)	EPBBF1	6210
Total Word Count (Document A) 0				
Total Word Count (Document B) 12831				
Total Word Count (All Documents) 12831				

Specification: ...reserve memory areas (the next available memory area) and a new memory, either primary or **secondary** depending upon which **memory** experience the malfunction or error, is generated to be used as a working alternate for... ...the memory device, the size of the memory area required for the program and how **many** usable memory areas maybe sectioned out of the overall **memory device**.

Although other **data** locating systems may be used, the practice of locating a particular register on the basis... ...own individual identifying number. By using a table of sequential hexadecimal numbers, each byte or **address may** be individually identified and located in its sequence of **location** in the **memory** bank, from the first byte to the last byte with its order of location corresponding... ...offset number would be limited to a range of numbers less than the differential between **successive** block **addresses**.

When the present invention is practiced using an accounting system employing first and second sets...other register, which may constitute the set or records or data, may each be positioned **at** some desired **location** within a **memory** block such as at predetermined offsets from the **address** of **the memory** block. Any **offset**, however, must be less than the address differential. Assume the offset of the ascending register... ...30. The address of the primary ascending register would be 255 + 30 or 285. The **address** of the **secondary** ascending register would be 509 + 30 or 539. The offset of the descending register may... ...the address of the primary descending register would be 255 + 60 or 315 while the **address** of the **secondary** descending register would be 509 + 60 or 569. The block address plus the offset for...

Dialog eLink: Order File History
8/3K/7 (Item 1 from file: 349)
DIALOG(R)File 349: PCT FULLTEXT

00877675

REPLICABLE PROBE ARRAY
RESEAU DE SONDE QUI PEUT ETRE DUPLIQUE

Patent Applicant/ Patent Assignee:

- **SURMODICS INC**
  9924 West 74th Street, Eden Prairie, MN 55344; US; US(Residence); US(Nationality)

Inventor(s):

- **GUIRE Patrick E**
  6741 Tartan Curve, Eden Prairie, MN 55346; US
- **SWANSON Melvin J**
  5290 Mount Carmel Road, Carver, MN 55315; US

Legal Representative:

- **DAIGNAULT Ronald A (agent)**
  Merchant & Gould P.C., P.O. Box 2903, Minneapolis, MN 55402-0903; US

	Country	Number	Kind	Date
Patent	WO	200210450	A2-A3	**20020207**
Application	WO	2001US21607		20010709

	Country	Number	Kind	Date
Priorities	US	2000631139		20000802

Designated States: (Protection type is "Patent" unless otherwise stated - for applications prior to 2004)
AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG,
BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ,
DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD,
GE, GH, GM, HR, HU, ID, IL, IN, IS, JP,
KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT,
LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ,
NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI,
SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ,
VN, YU, ZA, ZW

[EP] AT; BE; CH; CY; DE; DK; ES; FI; FR; GB;
GR; IE; IT; LU; MC; NL; PT; SE; TR;

[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GW; ML;
MR; NE; SN; TD; TG;

[AP] GH; GM; KE; LS; MW; MZ; SD; SL; SZ; TZ;
UG; ZW;

[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Language Publication Language: English
Filing Language: English
Fulltext word count: 23698

Detailed Description:

...10,000.

In a preferred embodiment of the invention, the master array support surface contains **redundant address** oligonucleotides immobilized thereon, such that a particular **address** appears at a **plurality** of spatially-defined **locations** on the master **array**. As a result of this redundancy, a particular multi-figand conjugate containing the complementary sequence...

Dialog eLink: Order File History
8/3K/8 (Item 2 from file: 349)
DIALOG(R)File 349: PCT FULLTEXT

00732562

REPLICABLE PROBE ARRAY
RESEAU DE SONDES REPLICABLES

Patent Applicant/ Patent Assignee:

- **SURMODICS INC**
  9924 West 74th Street, Eden Prairie, MN 55344; US; US(Residence); US(Nationality)

Inventor(s):

- **GUIRE Patrick E**
  6741 Tartan Curve, Eden Prairie, MN 55346; US

- **SWANSON Melvin J**
  5290 Mount Carmel Road, Carver, MN 55315; US

Legal Representative:

- **BRUESS Steven C**
  Merchant & Gould P.C., P.O. Box 2903, Minneapolis, MN 55402-0903; US

	Country	Number	Kind	Date
Patent	WO	200044939	A1	**20000803**
Application	WO	2000US1944		20000127
Priorities	US	99240466		19990129

Designated States: (Protection type is "Patent" unless otherwise stated - for applications prior to 2004)
AU, CA, JP, MX

[EP] AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LU; MC; NL; PT; SE;

Language Publication Language: English
Filing Language: English
Fulltext word count: 14172

Detailed Description:

...surface.

In a particularly preferred embodiment of the invention, the master array support surface contains **redundant address** oligonucleotides immobilized thereon, such that a particular **address** appears at a **plurality** of spatially-defined **locations** on the master **array**. As a result of this redundancy, a particular multi-ligand conjugate containing the complementary sequence...

Dialog eLink: Order File History
8/3K/9 (Item 3 from file: 349)
DIALOG(R)File 349: PCT FULLTEXT

00554384

REDUNDANT FORM ADDRESS DECODER FOR MEMORY SYSTEM
DECODEUR D'ADRESSE A FORME REDONDANTE POUR SYSTEME DE MEMOIRE

Patent Applicant/ Patent Assignee:

- **INTEL CORPORATION**

Inventor(s):

- **SAGER David J**

	Country	Number	Kind	Date
Patent	WO	200017757	A2	**20000330**
Application	WO	99US27873		19990827
Priorities	US	98148314		19980904

Designated States: (Protection type is "Patent" unless otherwise stated - for applications prior to 2004)
BR, CN, KR, SG, AT, BE, CH, CY, DE, DK,
ES, FI, FR, GB, GR, IE, IT, LU, MC, NL,
PT, SE

Language Publication Language: English

Fulltext word count: 6469

English Abstract:

The present invention provides a memory system (200) that retrieves data based upon **redundant** form **address** data. The memory system (200) includes a memory (220) having a plurality of memory lines... ...address decoder (210) that enables one of the memory lines (222) in response to a **redundant** form **address** signal. A **redundant** form decoder (230) decodes redundant form data into a differential pair of decoded address lines for each bit **position** of a **memory address**. One of the **two** differential pairs carries correct address data. The one address line to be used is determined... ...memory line by memory line basis, using the address of the memory lines themselves. The **redundant** form **address** decoder (230) avoids a completion add that would otherwise be required, yielding very fast access...

Claims:

...associated with an address of a predetermined width, an address decoder having an input for **redundant** form **address** signals, the address signals representing address data of data within the memory, the address decoder... ...the memory by enable lines. I 11. The memory system of claim 10, wherein the **redundant** form **address** data includes a **redundant** form data for every bit **position** of the **memory address** and for **two** n-1 bit positions adjacent to a least significant bit **position** of the **memory** address.
12 The memory system of claim I 1, wherein the memory lines are organized... ...data at the two bit positions.

13 The memory system of claim 10, wherein the **address** decoder comprising:
a **redundant** form decoder coupled to the inputs, anda memory driver coupled to the redundant form... ...each memory line associated with anaddress of a predetermined width, the method comprising:receiving **redundant** form **address** data for each bit **position** of the **memory address** and at least **two** bit positions below a least significant bit **position** of the**memory address**,decoding the **redundant** for **address** data, anddriving a first block and a second block based on the decoded address...

?